Amendments to the Specification

The following amendments to the specification are being made for consistency and are supported by the text and Figures of the original specification.

Please replace paragraph [0041] with the following amended paragraph:

[0041] For columns of memory cells not between the faulty column of memory cells and the redundant column of memory cells and the columns of memory cells in other memory arrays, the fault signal is not activated. The first and second multiplexers of these columns receive the redundancy implementation signal and the inactive fault signal. The multiplexers associated with these columns transfer the data signals from the input/output circuits ~~are transferred between~~ to their associated columns of memory cells.

Please replace paragraph [0043] with the following amended paragraph:

[0043] Refer now to Figs. 3, 4, and 5 for a more detailed discussion of the integrated circuit memory with a yield enhancement circuit of this invention. In this illustration, the memory is constructed of two arrays of memory cells **205** and **210**. Within the two memory arrays **205** and **210**, sub-arrays **215a, 215b, ..., 215z and 220a, ..., 220z** are composed of columns **225a, ..., 225z of memory cells 230a, 230b, ..., 230z**. A redundant column **235** of memory cells **240a, 240b, ..., 240z** is positioned to be associated with the memory arrays **205** and **210**. Each of the columns **225a, ..., 225z of memory cells 230a, 230b, ..., 230z** is connected to one read/write buffer circuit **255a, ...**

25[[45]]z. The redundant column 235 of memory cells 240a, 240b, ..., 240z is connected to its own read/write buffer 275.

Please replace paragraph [0045] with the following amended paragraph:

[0045] In the prior art, the read write buffer circuits are connected to be in direct communication with the associated input/output circuit. In the memory integrated circuit of this invention, the input and output ports of each of the read/write buffer circuits 225a, ..., 255m, 255n, ... 255z is connected respectively to the multiplexer-Input/Output circuit (MUX I/O) 450a, ..., 450z. Fig. 4 shows the internal components of a typical multiplexer-Input/Output circuit 450. Designations in Fig 4, such as 410 (iohit), 451 (READ n+1), 453 (READ n), 455 (WRITE n), 457 (WRITE from n-1) and 459 (WRITE to n+1) have corresponding designations for specific MUX I/O circuit blocks shown in Fig. 3. For example, corresponding signals for MUX I/O 450a are 410a, 451a, 453a, 455a, and 459a respectively. Referring to Fig. [[4]]3, each of the ~~the~~ input ports 455a, ...455z of each of the read/write buffer circuits 255a, ..., 255m, 255n, ... 255z~~of~~ ~~Fig. 3~~ is connected to an output 455a, ... , 455m, 455n, ... 455z of an associated MUX I/O, 450a, ..., 450m, 450n, ... 450z. As shown in Fig. 4, output 455 of each MUX I/O 450 is generated by first multiplexer 300. Each of output ports 453a, ..., 453z of each of the read/write buffer circuits 255a, ..., 255m, 255n,... 255z of Fig. 3 is connected to the respective primary input 453a, ..., 453m, 453n, ... 453z of a second multiplexer (shown

in detail in Fig. 4 as **295**), which is an element of each respective MUX I/O **450a, ..., 450m, 450n,... 450z**. Referring to Fig. 4, tThe secondary input **451 (READ n+1)** (represented by **451a, 451b, ... 451m, 451n, ... 451z** in Fig. 3) of the second multiplexer **295** is connected to signal **453 (READ n)**, which is shown in Fig. 4 for each MUX I/O depicted there as the output ports **453a, ..., 453z** of each of the read/write buffer circuits **255a, ..., 255m, 255n, ... 255z** of an adjacent column **225a, ..., 225z** of memory cells **230a, 230b, ..., 230z** or an adjacent sub-array **215a, 215b, ..., 215z and 220a, ..., 220z** of Fig. 3. Each MUX I/O **450a, 450b, ..., 450m, 450n,... 450z** contains aAn input/output circuit **260** (shown in Fig. 4)is associated with each sub-array **215a, 215b, ..., 215z and 220a, ..., 220z** of Fig. 3. As shown in a typical MUX I/O in Fig. 4, tThe input **265 (DQx)** (represented by **265a, 265b, ... 265m, 265n, ... 265z** in Fig.3) from external circuits as received by the input/output circuit **260** is transferred to the primary input of the first multiplexer **300** and as an output **459** of the multiplexer-Input/Output circuit **450**. The output e.g. **459** of one MUX I/O (e.g. **450a** in Fig 3) is connected~~, ..., 450z~~ to the secondary input **457 (WRITE from n-1)** of the first multiplexer **300** of a multiplexer-Input/Output circuit **450a, ..., 450z** associated with an adjacent column or sub-array. For example, the output **459a** from MUX I/O **450a** is connected to the input (457 in Fig. 4) to adjacent MUX I/O **450b**~~225a, ..., 225z of memory cells 230a, 230b, ..., 230z~~ as shown in Fig 3.

Please replace paragraph [0046] with the following amended paragraph:

[0046] Each multiplexer-Input/Output circuit **450a, ..., 450z** (depictied in a typical case in Fig. 4 as 450) has a multiplex control circuit **285** connected to the first multiplexers **300** and second multiplexer **295**. The mutiplex control circuit **285** receives a redundancy implementation signal **(REDUN) 415** and the redundancy implementation signal **(iohit ~~x~~) 410**. Referring back to Fig. 5~~3~~, the fault signal of an associated fault indication device **250a, ..., 250m, 250n, ... 250z** generates a redundancy implementation signal **410a, 410b, 410c..., 410m, 410n, ..., 410x, 410y 410z (iohit ~~x~~0L, iohit 1L, iohit 2L, ..., iohit mL, iohit nR, ..., iohit 2R, iohit 1R, iohit 0R)**, shown as **410** in Fig. 4 that is applied to the multiplex control circuit **285** to generate the multiplex control signals **(neihit ~~x~~) 430** of Fig. 4 that determine whether data reads on line **265** come from line **453 (READ n)** or line **451 (READ n+1)** and whether data writes on line **265** go to line **455 (WRITE n)** or line **459 (WRITE to n+1)**. In other words, whetheter data reads and writes are made to and from the default column when there is no fault or to and from the adjacent column when there is a fault. For example whether data reads and writes on line **265a** (Fig.3) are made to and from leftmost column **225a** or the next adjacent column (not shown).~~the associated column of memory cells within sub-arrays 215a, 215b, ..., 215z and 220a, ..., 220z is used for the adjacent column of memory cells within the sub-arrays 215a, 215b, ..., 215z and 220a, ..., 220z is used to sense or store data transferred by the associated input/output circuit 260a, ..., 260m, 260n, ... 260z.~~

Please replace paragraph [0047] with the following amended paragraph:

[0047] Each of t~~T~~he fault indication devices **250a, ..., 250m, 250n, ... 250z** as shown in Fig. 5, have a fuse (F1) shown typically in block **250b** as **252** that is connected between the ground reference point and typical~~the~~ resistor **254**. The resistor **254** is connected between the power voltage source V_{DD} and the fuse **252**. The junction of the fuse **252** and the resistor **254** is the terminal ~~(iohitnx)~~ **405b** that provides the fault signal. If there is no fault in an associated column **225a, ..., 225z** of memory cells **230a, 230b, ..., 230z** of the sub-arrays **215a, 215b, ..., 215z and 220a, ..., 220z**, the fuse is intact and the fault signal is at an inactive state (0). Alternately, if there is a fault in an associated column **225a, ..., 225z** of memory cells **230a, 230b, ..., 230z** of the sub-arrays **215a, 215b, ..., 215z and 220a, ..., 220z**, the fuse is destroyed and the fault signal is at an active state (1). Each of the fault indication devices shown in Fig. 5 as **250a, ..., 250m, 250n, ... 250z** further has a logical combining circuit marked typically in block **250b** as **256** which combines the fault signal **405a, ..., 405m, 405n, ... 405z** of the present fault indication device **250a, ..., 250m, 250n, ... 250z** with the combined fault signal **410a, ..., 410m, 410n, ... 410z** of an adjacent fault indication device **250a, ..., 250m, 250n, ... 250z** that is in the direction opposite the redundant column **235** of memory cells **240a, 240b, ..., 240z** as shown in Fig. 3.

Please replace paragraph [0048] with the following amended paragraph:

[0048] Referringto Fig. 5, t~~T~~he logical combination of the fault signals **410m** and **410n** from each array **205** and **210** is applied to the fault detection circuit **280** (Y FUSE). The fault detection circuit **280** combines the logical combination of fault signals **410m** and **410n** to create the redundancy implementation signals **415a** and **415b**. The fault detection circuit **280** is connected to the multiplex control circuits **285a, 285b, 285c, ... 285m, 285n, ..., 285x, 285y, 285z (MUX CTRL a, MUX CTRL b, MUX CTRL c, ..., MUX CTRL m, MUX CTRL n, ..., MUX CTRL x, MUX CTRL y, MUX CTRL z)** to transfer the redundancy implementation signal **415a** to the multiplexer control circuit **285a, ..., 285m** for the left array **205** and the redundancy implementation signal **415b** to the multiplex control circuit **285n, ... 285z** for the right array **210**.

Please replace paragraph [0049] with the following amended paragraph:

[0049] Referring to Fig. 3, t~~T~~he read/write buffer **275** is connected to the multiplexer **305** that receives the input data signals from the adjacent input/output circuits **260~~m and 260n~~** of MUX I/O's 450m and 450n of the left array **205** and the right array **210**. The multiplexer **305** is connected to the multiplex control circuit **290** to receive the a redundancy signal **420** indicating the existence of a fault within one of the memory arrays **205** and **210** and the array selection switch signal **425** indicating which array **205** ~~and~~or **210** has the fault. The fault detection circuit **280** is connected to the multiplex control circuit **290** associated with the redundant column **235** of memory cells **240a, 240b, ..., 240z** to provide the redundancy implementation signals **415a** and **415b**.

Please replace paragraph [0050] with the following amended paragraph:

[0050] If there are no faults in the memory arrays **205** and **210**, the multiplex control circuits **285a, ..., 285m, 285n, ... 285z** for the first multiplexers **300** and second multiplexers **295** contained in respective MUX I/Os **450a, ..., 450m, 450n, ... 450z** are set such that the data signals are directly transferred between the sub-arrays **215a, 215b, ..., 215z** and **220a, ..., 220z** and their associated input/output circuits **260** contained in respective MUX I/Os **450a, ..., 450m, 450n, ... 450z**. However, if for instance, a column of the sub-array 1 **215b** (Fig. 3) has a fault, the fuse **252** within the fault indication circuit **250b** (Fig. 5) is destroyed to activate the fault signal **405b**. The logic combination circuit **256** provides a logical ORing of the fault signals from the fuse **252** and the adjacent fault indication circuit that is opposite the fault indication circuit **250b** from the redundant column **235** of memory cells **240a, 240b, ..., 240z**. The ORing of the fault signal activates a combined fault signal **410b**. The successive fault indication signals combine the combined fault signal **410b, ..., 410m** to generate the input **410m** to the fault detection circuit **280**. The left redundancy implementation signal **415a** is activated and the right redundancy implementation signal **415b** remains inactive, thus indicating that the fault exists in the left memory **205** (shown in Fig. 3).

Please replace paragraph [0051] with the following amended paragraph:

[0051] Referring to Fig. 5, t~~T~~he multiplex control circuit **285a** **(MUX CTRL a)** receives an inactive combined fault signal **410a** **(iohit 0L)** and an active redundancy implementation signal **415a**. The multiplex control circuit **285a** **(MUX CTRL a)** sets the multiplex control signal **(neihit a0) 430a** such that (referring now to Fig. 4, in a detail of a typical MUX I/O circuit) the first multiplexer **300a** and the second multiplexer **295a** transfer the data signals from the input/output circuit **260a** to signal line **455 (WRITE n)**. Referring now to Fig. 3, the output of **MUX I/O 450a, 455a** is connected to **R/W BUFFER 255a**, which is connected to its associated sub-array **(SUB ARRAY 0,) 215a**. In similar fashion, referring to Fig. 5, t~~T~~he combined fault signals **410b, ..., 410m** and the redundancy implementation signal **415a** are the inputs respectively to the multiplex control circuit**s** **285a~~b~~, ..., 285m** for the left array **205** (as shown in Fig. 3). In the ~~illustration~~example being described, these signals are active causing the multiplex control circuits **285b, ..., 285m** to set the multiplex control signals **(neihit ~~x~~1, ..., neihit m) 430b, 430c, ..., 430m** to cause the first multiplexers **300~~b, ..., 300m~~** and second multiplexers **295~~b, ..., 295m~~** in each of MUX I/O blocks **450b, ..., 450m** to transfer the data signals from the input/output circuits **260~~b, ..., 260m~~** in each of MUX I/O blocks **450b, ..., 450m** to and from the adjacent columns of the sub-arrays **215b, ..., 215z**. Corresponding multiplex control signals for the right array are **430n, ... 430x, 430y, 430z.** The multiplexers **295~~m~~**in **MUX I/O 450m** and **305** are set to transfer the data signals between the input/output circuit **260~~m~~** in **MUX I/O 450m** and the redundant column **235** of memory cells **240a, 240b, ..., 240z**.

Please replace paragraph [00041] with the following amended paragraph:

[0052] The redundancy implementation signal **415b** and the combined fault signals **410n, ... 410z** are not activated. The data signals from the input/output circuit **~~260n, ... 260z~~** in MUX I/O 450n ...450z are transferred between their associated columns of the sub-arrays **220a, ..., 220z**.